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10/585,512	07/10/2006	Tsutomu Sakakibara	071971-0660	4161

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EXAMINER	
SNYDER, ADAM J	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,512	SAKAKIBARA ET AL.	
	Examiner	Art Unit	
	Adam J. Snyder	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 15, and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 11/17/2009 has been considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 2, 15, and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima et al (US 6,437,766 B1) in view of Wang (US 2002/0080108 A1).

Claim 1, Matsushima (Fig. 1 and 2) discloses a drive device (Fig. 1) comprising:

a first generation section (11-1 through 11-257; wherein elements produce signals P1-P256) for sequentially turning k first signals (P1-P256; wherein k is 256) from a non-output state to an output state (wherein figure 2 shows P1-P156 going from a non-output state to output state) according to a first clock (Fig. 2; wherein CLK is used to generate signals P1-P256 sequentially), where k is a natural number (wherein 256 is a natural number);

a second generation section (Col. 9, Line 6-8; wherein produces signals G1-G4) for sequentially turning m second signals (G1-G4; wherein m is 4) from the non-output

state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to a second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4), where m is a natural number (wherein 4 is a natural number); and

(k×m) (Col. 9, Lines 3-5; GP1-GP1024) output circuits divided into k groups (wherein figure 1 shows 256 groups),

wherein m output circuits (12-1 through 12-1056) belong to each of the k groups (wherein figure 1 shows four AND gates are connected to each of the 256 groups),

the k first signals (P1-P156) correspond to the k groups (wherein figure 1 shows P1-P256 connected to 256 groups),

the m second signals (G1-G4) correspond to the m output circuits (12-1 through 12-1056) belonging to each of the k groups (wherein figure 1 shows G1-G4 connected to 256 groups), and

each of the (k×m) (Col. 9, Lines 3-5; GP1-GP1024) output circuits:

outputs its corresponding second signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output circuit belongs is in the output state (Fig. 2; wherein figure 2 shows when both G1 and P1 is high out GP1 is high), and

does not output its corresponding second signal even when the second signal is in the output state if the first signal corresponding to the group to which the output circuit belongs is in the non-output state (Fig. 2; wherein figure 2 shows when G1 is high and P2 is low then GP5 is not output).

Matsushima does not expressly disclose wherein the first generation section includes k first level shifters outputting the k first signals after shifting a voltage level of the k first signals from a first voltage level used in the first generation section to a second voltage level used in the output circuits,

the second generation section includes m second level shifters outputting the m second signals after shifting a voltage level of the m second signals from a first voltage level used in the second generation section to a second voltage level used in the output circuits.

Wang (Fig. 3-5) discloses wherein the first generation section (SR_1-SR_K) includes k first level shifters (LSD_1-LSD_K) outputting the k first signals (D1-DK) after shifting a voltage level of the k first signals from a first voltage level used in the first generation section to a second voltage level used in the output circuits (Paragraph [0026]; 32; Fig. 4),

the second generation section (Paragraph [0027]) includes m second level shifters (LSC_1-LSC_L) outputting the m second signals (C1-CL) after shifting a voltage level of the m second signals from a first voltage level used in the second generation section to a second voltage level used in the output circuits (Paragraph [0027]; 32; Fig. 4).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima's scan driving circuit by applying level shifters, as taught by Wang, so to use a scan driving circuit with level shifters for providing a new driving circuit for the gate control lines and a method to efficiently

decrease the number of level shifters needed and consequently reduce the cost of LCD manufacture (Paragraph [0012]).

Claim 15, Matsushima (Fig. 1 and 2) discloses a drive method (Fig. 2) for sequentially outputting drive signals (GP1-GP1024) from (k×m) output terminals divided into k groups (wherein figure 1 shows 256 groups), where k and m are natural numbers (wherein 256 and 4 are natural numbers), m output terminals (wherein 4 output terminals GP1-GP1024 belong with each group) belonging to each of the k groups (wherein figure 1 shows 256 groups), the method comprising:

sequentially turning k first signals (Fig. 2; P1-P256; wherein k is 256) corresponding to the k groups (wherein figure 1 shows 256 groups) from a non-output state to an output state (wherein figure 2 shows P1-P156 going from a non-output state to output state) according to a first clock (Fig. 2; wherein CLK is used to generate signals P1-P256 sequentially);

sequentially turning m second signals (Fig. 2; G1-G4; wherein m is 4) corresponding to the m output terminals (12-1 through 12-1056) belonging to each of the k groups (wherein figure 1 shows four AND gates are connected to each of the 256 groups) from the non-output state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to a second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4); and

in each of the (k×m) output terminals (Col. 9, Lines 3-5; GP1-GP1024), outputting the second signal corresponding to the output terminal from the output terminal as the drive signal when the second signal is turned to the output state if the first signal corresponding to the group to which the output terminal belongs is in the output state (Fig. 2; wherein figure 2 shows when both G1 and P1 is high out GP1 is high); and

in each of the (k×m) output terminals (Col. 9, Lines 3-5; GP1-GP1024), not outputting the second signal corresponding to the output terminal from the output terminal as the drive signal even when the second signal is in the output state if the first signal corresponding to the group to which the output terminal belongs is in the non-output state (Fig. 2; wherein figure 2 shows when G1 is high and P2 is low then GP5 is not output).

Matsushima does not expressly disclose shifting a voltage level of the k first signals from a first voltage level corresponding to the first clock to a second voltage level corresponding to the drive signals;

shifting a voltage level of the m second signals from a first voltage level corresponding to the second clock to a second voltage level corresponding to the drive signals.

Wang (Fig. 3-5) discloses shifting a voltage level (LSD_1-LSD_K) of the k first signals (SR_1-SR_K) from a first voltage level corresponding to the first clock (Fig. 5; wherein the figure shows D1-DK being produced at a first clock signal) to a second voltage level corresponding to the drive signals (Paragraph [0026]; 32; Fig. 4);

shifting a voltage level (LSC_1-LSC_L) of the m second signals (Paragraph [0027]) from a first voltage level corresponding to the second clock (Fig. 5; wherein the figure shows C1-CL being produced at a second clock signal) to a second voltage level corresponding to the drive signals (Paragraph [0027]; 32; Fig. 4).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima's scan driving circuit by applying level shifters, as taught by Wang, so to use a scan driving circuit with level shifters for providing a new driving circuit for the gate control lines and a method to efficiently decrease the number of level shifters needed and consequently reduce the cost of LCD manufacture (Paragraph [0012]).

Claim 2, Matsushima (Fig. 1 and 2) discloses wherein the second generation section sequentially turns the m second signals (Col. 9, Line 6-8; wherein produces signals G1-G4) from the non-output state to the output state (wherein figure 2 shows G1-G4 going from a non-output state to output state) according to the second clock (Fig. 2; wherein T is used to generate signals G1-G4 sequentially; Col. 9, Line 66-Col. 10, Line 4) during the time when any one of the k first signals is in the output state (wherein figure 2 shows producing signals G1-G4 during any one of P1-P256 signals).

Claim 16, Wang (Fig. 5 and 6) disclose wherein the first clock (Fig. 5; wherein the first clock signal is used to generate C1-CL) is a clock obtained by (Fig. 6; wherein

figure 6 shows process for the second clock signal to driving the first clock signal) the second clock (Fig. 5; wherein the first clock signal is used to generate D1-DK).

4. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima et al (US 6,437,766 B1) in view of Wang (US 2002/0080108 A1) as applied to claim 1 above, and further in view of Murakami et al (JP 05-313129 A).

Claim 3, Matsushima in view of Wang discloses the drive device of Claim 1.

Matsushima in view of Wang does not expressly disclose wherein each of the (k×m) output circuits includes:

an output terminal;

a first input terminal for receiving the second signal corresponding to the output circuit;

a first switch connected between the output terminal and the first input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit;

a second input terminal for receiving a predetermined voltage corresponding to the non-output state of the second signal, and

a second switch connected between the output terminal and the second input terminal for switching ON/OFF according to the state of the first signal corresponding to the output circuit.

Murakami (Fig. 8, 1, 2, 5, and 9) discloses wherein each of the (k×m) output circuits (Fig. 9a and 9b) includes:

an output terminal (OUT);

a first input terminal (A) for receiving the second signal (V1) corresponding to the output circuit (Fig. 2);

a first switch (Te or Tg) connected between the output terminal (OUT) and the first input terminal (A) for switching ON/OFF (Paragraph [0010]; wherein Sc controls out state input terminals) according to the state of the first signal (Sc) corresponding to the output circuit (Fig. 2);

a second input terminal (B) for receiving a predetermined voltage (i.e. ground) corresponding to the non-output state of the second signal (wherein second terminal is selected and while not outputting the second signal), and

a second switch (Tf or Th) connected between the output terminal (OUT) and the second input terminal (B) for switching ON/OFF (Paragraph [0010]; wherein Sc controls out state input terminals) according to the state of the first signal (Sc) corresponding to the output circuit (Fig. 2).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima in view of Wang's gate control device by applying an output control circuit, as taught by Murakami, so to use a gate control device with an output control circuit for providing a high definition display, without increasing substantially the number of lessening the number of scan driver IC and attaining low-pricing, or scan driver IC (Paragraph [0006]).

5. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima et al (US 6,437,766 B1) in view of Wang (US 2002/0080108 A1) as applied to claim 1 above, and further in view of Morita (US 7,079,122 B2).

Claim 4, Matsushima in view of Wang discloses the drive device of Claim 1.

Matsushima in view of Wang does not expressly disclose wherein the first generation section includes k first flipflops connected in series, and

the second generation section includes m second flipflops connected in series.

Morita (Fig. 14) discloses wherein the first generation section includes k first flipflops connected in series (FFB0-FFBQ; wherein each block contains one control flip-flop), and

the second generation section includes m second flipflops connected in series (FF1-FF8; wherein each block contains eight row control flip-flips).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Matsushima in view of Wang's gate control device by using flip-flops, as taught by Morita, so to use a gate control device with flip-flops for driving the plurality of scan lines sequentially in a designated block at the time of the partial display mode produces a high image quality and a low power consumption compatibility (Col. 3, Lines 37-42; Col. 2, Lines 30-31).

Response to Arguments

6. Applicant's arguments with respect to claims 1-4, 15, and 16 have been considered but are moot in view of the new ground(s) of rejection.

In view of arguments, the references of Matsushima et al (US 6,437,766 B1), Wang (US 2002/0080108 A1), Murakami et al (JP 05-313129 A), and Morita (US 7,079,122 B2) have been used for new ground rejection.

Claims 1 and 15 are rejected in view of newly discovered reference(s) to Wang (US 2002/0080108 A1).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam J. Snyder whose telephone number is (571) 270-3460. The examiner can normally be reached on M-F (8:30am-5pm) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AJS/
Examiner, Art Unit 2629
01/27/2010

/Chanh Nguyen/
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